REMARKS

Applicants thank the Examiner for the thorough consideration given the present application.

Claims 1-3, 5, 7-10, 12, and 15 are pending. Claims 4, 6, 11, 13, 14, 16, and 17 are canceled. Claims 1, 2, 5, 8-10, 12, and 15 are amended. Claims 1 and 9 are independent.

Reconsideration of this application, as amended, is respectfully requested.

Claim for Priority

Applicants thank the Examiner for acknowledging their claim for foreign priority under 35 U.S.C. §119 and receipt of the certified copy of the priority document.

Drawings

The Examiner is requested to approve the proposed drawing changes filed January 28, 2002, and to provide a Notice of Draftsperson's Patent Drawing Review, Form PTO-948, with the next official communication.

Rejection under 35 U.S.C. §112, second paragraph

Claims 1-17 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. This rejection is respectfully traversed.

As the Office Action indicates, power consumption by the memory device is detected from a level of the boosted voltage (VPP) outputted form the charge pump circuit. In other words, if power consumption by the memory device increases, the level of the boosted voltage (VPP) is lowered. On the other hand, if power consumption by the memory device decreases, the level of the boosted voltage (VPP) becomes high. Accordingly, if the boosted voltage (VPP) becomes high enough and all the voltages (DIV2-DIVn), except for the voltage (DIV1), are higher than the reference voltage (VREF), the charge pumps (second to nth) are not driven. Here, the voltage (DIV1) is always lower than the reference voltage (VREF). Thus, the charge pump is always driven.

If the boosted voltage (VPP) decreases and then the voltages (DIV2-DIVn) become sequentially lower than the reference voltage (VREF), the charge pumps (second to nth) are sequentially driven. Thereafter, the boosted voltage (VPP) becomes low enough so that all of the voltages (DIV1-DIVn) are lower than the reference voltage (VREF). Thus, all of the charge pumps (first to nth) are driven.

It appears there may be some confusion regarding the operation of the differential amplifier in the multilevel

detector (100). As shown in FIG. 4, the first differential amplifier 100-1 receives the lowest voltage (DIV1) and generates a signal (DET1) to drive the first charge pump (40-1). However, the voltage (DIV1) is always lower than the reference voltage (VREF). NMOS transistors are turned on by the reference voltage (VREF) and the pumping enabling signal (PUMP_ON). Since the voltage level of the output terminal of the first differential amplifier (100-1) becomes low, the low level voltage becomes the high level voltage (DET1) by inverting through an inverter.

In addition to the foregoing explanation, the specification and claims are amended to replace "step-up voltage" with "boosted voltage" and to change "host" to "memory device." In view of the preceding discussion and amendments herein, it is believed that the claims are clear and definite, and reconsideration and withdrawal are requested of the rejection under 35 U.S.C. §112, second paragraph.

Rejections under 35 U.S.C. §102(b)/§103(a)

Claims 1-5, 9, and 13-15 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,128,242 to Banba et al., and claims 16 and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Banba et al. These rejections are respectfully traversed.

While not conceding the appropriateness of the rejections, but merely to advance prosecution of the present application, independent claim 1 is amended to incorporate the canceled subject matter of claim 6, and independent claim 9 is amended to incorporate the canceled subject matter of claims 11 and 14.

It is respectfully submitted that the combinations of steps and elements set forth in the independent claims are not disclosed or made obvious by the prior art of record, including Banba et al.

As shown in FIG. 8, Banba et al. merely shows a power supply circuit including an oscillator 21, booster circuits 22 to 25, operational amplifiers 27 and 28, AND gates 30-32, and inverter 33.

However, Banba et al. does not teach or suggest a voltage distributor for dividing a boosted voltage into first to nth voltage levels and first to nth voltage level detectors for detecting a plurality of levels of the boosted voltage by comparing the first to nth levels divided by the voltage distributor with a reference level, as recited in claims 1 and 10, and first to nth level detectors including a differential amplifier, as recited in claims 7 and 9.

In view of the foregoing, it is respectfully submitted that Banba et al. fails to anticipate or render obvious the present

invention, and reconsideration and withdrawal are requested of the rejections under 35 U.S.C. §102(b) and §103(a). Independent claims 1 and 9 are believed to be in condition for allowance. Since the remaining claims depend directly or indirectly from these allowable independent claims, they should also be allowable for at least the reasons set forth above, as well as for the additional limitations provided thereby. Therefore, all pending claims should be in condition for allowance.

CONCLUSION

Since the remaining patents cited by the Examiner have not been utilized to reject claims, but merely to show the state of the art, no comment need be made with respect thereto.

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

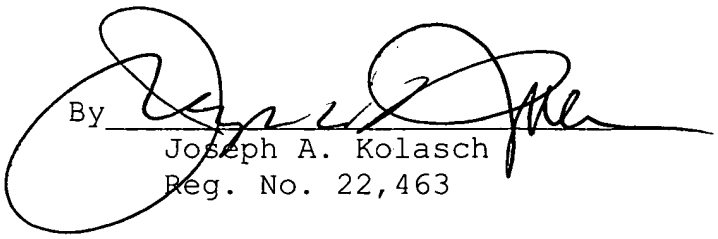
Should any issues remain, however, the Examiner is invited to telephone Sam Bhattacharya (Reg. No. 48,107) at (703) 205-8000 in an effort to expedite prosecution.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit

any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP



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ABSTRACT OF THE DISCLOSURE

A charge pump device for supplying a [step-up] boosted voltage to a [host,] memory device includes[:] a charge pump part constructed with first to nth unit charge pumps, and a multi-level detector for detecting a level of a [step-up] boosted voltage to selectively drive the unit charge pumps in accordance with an amount of power consumption of the host and thereby outputting at least one level detection signal.

MARKED-UP COPY OF AMENDMENTS

IN THE SPECIFICATION:

Please **rewrite paragraph [02]** as follows:

[02] The present invention relates to a circuit for generating a [step-up] boosted voltage in a semiconductor memory, and more particularly, to a charge pump circuit in a semiconductor memory.

Please **rewrite paragraph [04]** as follows:

[04] Referring to Fig. 1, the charge pump circuit 50 is constructed with a level detector 10 for detecting a level of a [step-up] boosted voltage VPP by comparing it with a reference voltage VREF and producing a level detection signal DET based on the comparison results, an oscillator 20 for producing a pulse signal PUL in accordance with the level detection signal DET output from the level detector 10, and a charge pump unit 30 for outputting a [step-up] boosted voltage VPP by carrying out a charge pumping operation in accordance with the pulse signal PUL output from the oscillator 20. The charge pump unit 30 comprises at least one of a plurality of unit charge pumps 30-1 to 30-n.

a multi-level detector [for detecting] that detects a level variation of [a step-up] the boosted voltage [to] and outputs a plurality of level detection signals for selectively [drive] driving the unit charge pumps [in accordance with an amount of power consumption of the host and thereby outputting at least one level detection signal], the multi-level detector including:

a voltage distributor for dividing the boosted voltage into first to nth voltage levels; and

first to nth level detectors for comparing the first to nth voltage levels with a reference level and generating the first to nth level detection signals.

2. (Amended) The [change] charge pump device of claim **1**, further comprising:

an oscillator for producing a pulse signal in accordance with the first level detection signal [of] from the [multi-level] first level detector; and

a logic operation part for [performing a logic operation on] logically operating the pulse signal of the oscillator and the second to nth level detection signal [produced] from the [multi-level detector] second to nth level detectors, and outputting the operated signal to the charge pump part.

5. (Amended) The charge pump device of claim 1, wherein the second to nth unit charge [pump is] pumps are selectively driven [when the amount of power consumption by the host is low] in accordance with the level of the boosted voltage when the memory device is operated in an active state.

8. (Amended) The charge pump device of claim [6] **1**, wherein the first voltage level is always lower than the reference level.

9. (Amended) A charge pump device associated with a [host] memory device, comprising:

a charge pump part including first to nth unit charge pumps to generate a boosted voltage;

a multi-level detector [detecting] that detects a level of [a step-up] the boosted voltage [so as] and outputs first to nth level detection signals for selectively [drive] driving the unit charge pumps [in accordance with an amount of power consumption of the host], wherein the first unit charge pump is always driven by the first level detection signal output from the multi-level detector, and each of the first to nth level detectors is composed of a different amplifier[;

a signal generator producing a pulse signal in accordance with a level detection signal of the multi-level detector; and

a logic operation part operating on the pulse signal of the oscillator and the level detection signal produced from the multi-level detector, and thereby outputting an operated signal to the first to nth unit charge pumps].

10. (Amended) The charge pump device of claim **9**, wherein the multi-level detector includes:

a voltage distributor for dividing [a power source] the boosted voltage into first to nth voltage levels; and

first to nth level detectors for detecting a plurality of levels of the [step-up] boosted voltage by comparing the first to nth voltage levels divided by the voltage distributor with a reference level.

12. (Amended) The charge pump device of claim **10**, wherein the first voltage level is always lower than the reference level.

15. (Amended) The charge pump device of claim **9**, wherein the second to nth unit charge [pump is] pumps are selectively driven in accordance with the level of the boosted voltage when the

[amount of power consumption by the host] memory device is [low] operated in an active state.

Please **rewrite paragraph [05]** as follows:

[05] [Figs.] Fig. 2 is a detailed circuit diagram of the level detector 10 in Fig. 1. As shown in Fig. 2, the level detector 10 is constructed with a differential amplifier for comparing the [step-up] boosted voltage VPP to the reference voltage VREF and outputting the level detection signal DET. A pumping enabling signal PUMP_ON is input to a gate of an NMOS transistor NM3.

Please **rewrite paragraph [07]** as follows:

[07] When the charge pump circuit 50 is operated by a high level stage of the pumping enabling signal PUMP_ON, the level detector 10 detects a level of the [step-up] boosted voltage VPP by comparing a VPP level to the reference voltage VREF. Namely, as shown in Fig. 2, if the level of the reference voltage VREF is higher than the level of the [step-up] boosted voltage VPP, the level detector 10 outputs a level detection signal DET of a high level through an inverter INV. If the level of the reference voltage VREF is lower than the level of the [step-up] boosted voltage VPP, a level detection signal DET of a low level is output by the level detector 10.

Please **rewrite paragraph [14]** as follows:

[14] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a charge pump circuit in a semiconductor memory according to an embodiment of the present invention, includes a charge pump unit constructed with a first to an nth unit charge pumps, a multi-level detector detecting a level of a [step-up] boosted voltage by multi-steps so as to drive the unit charge pumps variably in accordance with an amount of power consumption of the device, an oscillator producing a pulse signal in accordance with a detect signal of the multi-level detector, and a logic operation part operating the pulse signal of the oscillator and a level detect signal produced from the multi-level detector and outputting the operated signal to the charge pump unit.

Please **rewrite paragraph [15]** as follows:

[15] Preferably, the multi-level detector includes a voltage distributor dividing a power source voltage into a first to an nth voltage levels, and a first to an nth level detectors detecting the level of the [step-up] boosted voltage by

comparing the [step-up] boosted voltage to the first to nth voltage levels divided by the voltage distributor.

Please **rewrite paragraph [17]** as follows:

[17] In another aspect of the present invention, a charge pump circuit in a semiconductor memory includes a charge pump unit constructed with a first to an nth unit charge pumps, a multi-level detector detecting a level of a [step-up] boosted voltage by multi-steps so as to drive the unit charge pumps variably in accordance with an amount of power consumption of the device, an oscillator producing a pulse signal in accordance with a detect signal of the multi-level detector, and a logic operation part operating the pulse signal of the oscillator and a level detection signal produced from the multi-level detector, the logic operation part outputting the operated signal to the first to nth unit charge pumps, wherein the multi-level detector comprises a voltage distributor dividing a power source voltage into a first to an nth voltage levels, and a first to an nth level detectors detecting a plurality of levels of the [step-up] boosted voltage by comparing the [step-up] boosted voltage to the first to nth voltage levels divided by the voltage distributor.

Please **rewrite paragraph [27]** as follows:

[27] Referring to Fig. 3, the charge pump device 500 is constructed with a multi-level detector 100 for detecting a level of a [step-up] boosted voltage VPP using multiple steps, an oscillator 200 for producing a pulse signal PUL in accordance with a first level detection signal DET1 detected by the multi-level detector 100, a charge pump part 400, and a logic operation part 300 for driving the charge pump part 400 by NANDing both the pulse signal PUL of the oscillator 200 and second to nth-level detection signals DET2 to DETn detected by the multi-level detector 100. The elements are all operatively connected.

Please **rewrite paragraph [29]** as follows:

[29] Fig. 4 is a circuit diagram of the multi-level detector 100 in Fig. 3 according to one embodiment of the present invention. As shown in Fig. 4, the multi-level detector 100 is constructed with a voltage distributor 101 for dividing a power source voltage into a plurality of voltage levels DIV1 to DIVn each corresponding to a divided [step-up] boosted voltage, and a plurality of level detectors 100-1 to 100-n each detecting a level of a divided [step-up] boosted voltage by comparing the

reference voltage VREF to the corresponding one of the divided voltage levels DIV1 to DIVn. A pumping enabling signal PUMP_ON is applied to an NMOS gate in each of the level detectors 100-1 to 100-n, which generates and outputs a level detection signal DET1...DETn based on the level detection results. In this case, the level detectors 100-1 to 100-n are implemented by using a differential amplifier (e.g., composed of PMOS and NMOS transistors) that are preferably not affected by a process variation, temperature, or other factors. But, the implementation of the level detectors 100-1 to 100-n is not limited to such, but can be made using other means.

Please **rewrite paragraph [31]** as follows:

[31] As shown in Figs. 5A-5B, when a pumping enabling signal PUMP_ON is at a high level by power-on of an apparatus, system or the like **[**(host)**]** (memory device) associated with the device 500, the multi-level detector 100 outputs first to nth level detection signals DET1 to DETn by comparing a VPP level to the reference voltage VREF. At this time, all of the first to nth level detection signals DET1 to DETn are at a high level since the initial level of the **[**step-up**]** boosted voltage VPP output from the charge pump part 400 is low.

Please **rewrite paragraph [32]** as follows:

[32] Subsequently, the oscillator 200 generates and outputs a pulse signal PUL in accordance with the high level detection signal DET1. The pulse signal PUL output from the oscillator 200 is then applied to the charge pump part 400 through the logic operation part 300, thereby operating all of the first to nth unit charge pumps 40-1 to 40-n. Thus, the VPP level rises from low to high. Once the level of the [step-up] boosted voltage VPP rises, the multi-level detector 100 generates the first to nth level detection signals DET1 to DETn that have been switched from a high to low level due to the rising of the [step-up] boosted voltage VPP. The level detection signals DET1 to DETn at a low level then place the unit charge pumps 40-2 to 40-n in a standby state by reducing the number of the unit charge pumps 40-2 to 40-n that are in operation.

Please **rewrite paragraph [33]** as follows:

[33] Particularly, at the standby state, the level of the [step-up] boosted voltage VPP is maintained by operating only the first unit charge pump 40-1, which is possible by designing a level of the divided voltage DIV1 output from the voltage

distributor 101 to be lower than the reference voltage VREF based on this formula:

$$DIV1=VPP*R0/(R0+R1+\ldots+Rn)$$

where R0,R1...Rn are the values of resistors.

Please **rewrite paragraph [34]** as follows:

[34] When the associated apparatus (e.g., memory) starts to consume power at an active stage (low-speed operation), a level of the [step-up] boosted voltage VPP decreases. Once the level of the [step-up] boosted voltage VPP is decreased, the level of the divided voltage [DIV1] DIV2 to be compared with the reference voltage VREF decreases as well. Then, the second level detection signal DET2 output from the level detector 100-2 is shifted from a low level to a high level, whereby the second unit charge pump 40-2 starts to operate.

Please **rewrite paragraph [35]** as follows:

[35] Thereafter, if too much power is consumed by the device in the active stage (high-speed operation), the level of the [step-up] boosted voltage VPP is greatly lowered, whereby other detection signals such as the nth level detection signal DETn output from the level detector 100-n is shifted from low to high. In this manner, all of the first to nth level detection

signals DET1 to DETn can be selectively switched to a high level, thereby turning on all the unit charge pumps 40-1 to 40-n.

Please **rewrite paragraph [36]** as follows:

[36] By carrying out such procedures repeatedly to drive selectively one, two or more of the plurality of the unit charge pumps in accordance with the amount of power consumed by the apparatus (e.g., memory) or the like associated with the charge pump device 500, the charge pump device according to the present invention maintains the level of the **[**step-up**]** boosted voltage VPP. For example, one unit charge pump 40-1 is driven only at a standby stage, two unit charge pumps 40-1 and 40-2 may be driven at a low power consumption stage, and all or most of the unit charge pumps 40-1 to 40-n may be driven at a high power consumption stage.

Please **rewrite paragraph [37]** as follows:

[37] Accordingly, the charge pump device according to the present invention reduces power consumption by adjusting automatically the number of unit charge pumps in operation in accordance with the power consumption variation of an associated apparatus by detecting a level of a **[**step-up**]** boosted voltage.

IN THE ABSTRACT:

Please **amend the Abstract** as follows:

ABSTRACT OF THE DISCLOSURE

A charge pump device for supplying a [step-up] boosted voltage to a [host,] memory device includes[:] a charge pump part constructed with first to nth unit charge pumps, and a multi-level detector for detecting a level of a [step-up] boosted voltage to selectively drive the unit charge pumps in accordance with an amount of power consumption of the host and thereby outputting at least one level detection signal.

IN THE CLAIMS:

Please **cancel claims 4, 6, 11, 13, 14, 16, and 17** without prejudice or disclaimer.

Please **amend claims 1, 2, 5, 8-10, 12, and 15** as follows:

1. (Amended) A charge pump [device] circuit for supplying a [step-up] boosted voltage to a [host] memory device, [the device] comprising:

a charge pump part constructed with first to nth unit charge pumps; and